TOSHIBA

TC260 SLI ASIC Family with Embedded DRAM 0.14µm/1.5V

Description

The TC260 family of System-Level Integration (SLI) ASICs are designed for applications needing the highest performance with the smallest die size. The TC260 employs the highest-density interconnects, gates, memory, and I/O structures. The family includes TC260C/DC Standard Cells for best density or TC260E/DE Embedded Arrays for fast turnaround time. The 0.14µm drawn geometry is ideal for systems above 150MHz or 2Mgates and those applications requiring the lowest power dissipation. Two technology module options may also be employed, a Precision Analog Module for mixed-signal applications and a Performance Module for optimizing challenging timing paths.

Toshiba offers two types of embedded DRAM, one targeted for high-bandwidth, the other for SRAM replacement applications. The embedded DRAM cores are based on Toshiba's leading trench capacitor technology, which permits mixing of logic and DRAM without degrading logic performance. Toshiba's IP library includes a full line of MIPS® RISC and application-specific cores such as PCI, USB, 1394, AGP, SCSI, Fast Ethernet, etc. Toshiba's Timing-Driven Flow (TDF™) design methodology is based on commercial EDA tools and ensures that timing closure can be achieved typically with only a few simple ECOs.

TC260 Family Features

- 0.14µm drawn, 6-layer-metal CMOS process
- Over 125K usable gates/mm^2 (Standard Cell)
- Two types of I/O cell sizes
  - Narrow for pad-limited designs
  - Short for core limited designs
- 4.20µm^2 high-density SRAM cells with 512Kbits/block
- Two types of primitive cell libraries
  - Embedded Array for fast turnaround time
  - Standard Cell for highest density
- 36ps 2-input NAND gate delay @ 10ps input slew, fanout = 2 plus estimated wire length load (CND2 × 4)
- V_{DD} = 1.5V±10% (Core); 1.5V, 2.5V or 3.3V (I/O)
- Typical 2W power dissipation at 200MHz (36mm^2 die)
- Two technology module options
  - Precision 2.5V Analog module for mixed-signal applications
  - Performance module for optimizing challenging timing paths
- Comprehensive core and high-performance I/O cell library for SLI implementation
- Timing-Driven Flow (TDF) based on commercial EDA tool sign-off for design flexibility
- Wide range of package options including QFP, TBGA, FCBGA, and EPBGA with pin counts and performance to meet all application needs

TC260 Embedded DRAM Cores

- 2 types of DRAM cores
  - High-bandwidth, 200MHz regular SDRAM with 2–32Mb, 1–4 banks, and 64–256 bits wide per macrocell
  - Fast-Access DRAM with 12ns t_{RC}, 2/4/8Mb 256 bits macrocells
- Over 6.4GB/s macrocell bandwidth at 256bits wide
- Synchronous interface. All signals referenced to positive edge of clock
- Automatic refresh
- Byte Write data control
- Typical 62mm^2 die for 32Mb DRAM with 500K gates
- Typical 128mm^2 die for 64Mb DRAM with 1.5M gates
- 1-transistor cell structure utilizing trench capacitor technology

Embedded DRAM Benefits

- Flexibility in configuring the DRAM macrocell based on application requirements
- High bandwidth due to wide and fast memory busses
- Faster access time than discrete DRAMs
- Fewer external devices and reduction of total and ASIC pin count
- Lower power dissipation—systems with fast and wide memory busses will dissipate significantly less power due to lower-capacitance on-chip connections
- Lower switching noise on data bus between memory and logic

Toshiba Trench Capacitor Benefits

Benefits when compared to stacked capacitor technology are significant:

- Higher-density DRAM core and gate count for a given die size
- Logic transistor performance is not degraded by manufacturing the memory capacitor
- The trench capacitor, which is formed beneath the surface of the silicon, allows a planar silicon surface topology which improves reliability
- Low soft-error rates, since these larger capacitors require higher charges to change states

Toshiba TDF Flow Benefits

TDF is the only appropriate ASIC design methodology for 0.14µm technology. TDF is based on commercially available EDA tools. Using TDF results in reduced design cycle time by cutting iterations to often just a couple of place-and-route ECOs. Without TDF it is also not uncommon for over 10 layout iterations to still fail to meet timing specifications.

System-Level Packaging

The TC260 utilizes a compact 40mm I/O slot to accommodate the reduction of die size made possible by the 0.14µm technology. I/O cells are available in 1-slot wide by 540µm deep for pad-limited designs or 2-slots wide by 370µm deep for core-limited designs.

Toshiba's comprehensive package options include low-cost PQFPs and TBGAs (tape ball grid arrays), EBGAs (electrically enhanced ball grid arrays), and high-performance, high-pin-count FCBGAs (flip-chip ball grid arrays) offered with pin counts in the range of 500–1500 pins. Toshiba also offers fine-pitch BGAs (ball pitch <1.0mm) with pin counts in the range of 141–265 pins.

The TC260 is available in most other standard package options and pin counts. See our Package Availability Guide for a complete listing.

Application-Specific IP

Toshiba supports an ever-growing selection of IP cores in many technologies. These range from basic cells, such as RAM, ROM, register files, UART, A/D, D/A, and PLL, through application-specific IP, such as USB, IrDA, IEEE 1394, MAC 10/110, PCI controllers, RISC, SCSI, MPEG, QAM and QPSK. IP is developed by Toshiba, obtained from third-party partners, imported from other IP suppliers, or provided by customers. Contact Toshiba for detailed TC260 availability.

Technology Resource Centers

Toshiba SLI ASIC Technology Resource Centers are located throughout the U.S. to provide technical support before, during, and after the design of a Toshiba ASIC. This includes support with EDA environments and design kits, Toshiba design methodologies, ASIC technologies, and design implementation.

In addition, Toshiba's North America Semiconductor Engineering Development Center based in San Jose, CA is staffed with system, technology, and EDA design experts who work with customers on advanced System IC applications, and who can also provide complete design services.

High-Quality, High-Volume Manufacturing

Toshiba's ASIC manufacturing plants are among the largest and most advanced in the world. They are all certified to ISO9000. Rigorous quality control coupled with a sophisticated batch tracking system allows Toshiba to meet the needs of fast-ramping, high-volume markets.

TOSHIBA

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